REMARKS

In the Final Office Action, the Examiner rejected claims 1-14, 16-32 and 34-50. Applicant respectfully submits that all pending claims are in condition for allowance. Reconsideration of the application in view of the following remarks is respectfully requested.

Claim Rejections Under 35 U.S.C. § 103(a)

In the Final Office Action, the Examiner rejected claims 1, 6-10, 12-14, 23-25, and 46-48 under 35 U.S.C. § 103(a) as being unpatentable over Inagami et al., U.S. Patent No. 4,881,168 (hereafter referred to as "the Inagami reference"), and, in addition, Wright, et al., U.S. Patent No. 5,587,961 (hereafter referred to as "the Wright reference") is cited as extrinsic evidence for showing that precharge and deactivate commands exist. The Examiner also rejected claims 2-5, 11 and 26-27 under 35 U.S.C. § 103(a) as being unpatentable over the Inagami reference, as applied above, in view of Parady, U.S. Patent No. 5,933,627 (hereafter referred to as "the Parady reference"), and rejected claims 16-22, 28-32, 34-45 and 49-50 under 35 U.S.C. § 103(a) as being unpatentable over the Inagami reference in view of the Parady reference, as applied above, and further in view of Bissett et al., U.S. Patent No. 5,896,523 (hereafter referred to as "the Bissett reference"). Applicant respectfully traverses these rejections.

Legal Precedent

First, the pending claims must be given an interpretation that is reasonable and consistent with the *specification*. *See In re Prater*, 415 F.2d 1393, 1404-05, 162 U.S.P.Q. 541, 550-51 (C.C.P.A. 1969) (emphasis added); *see also In re Morris,* 127 F.3d 1048, 1054-55, 44 U.S.P.Q.2d 1023, 1027-28 (Fed. Cir. 1997); *see also* M.P.E.P. §§ 608.01(o) and 2111. Indeed, the specification is "the primary basis for construing the claims." *See Phillips v. AWH Corp.*, 415 F.3d 1303, 75 U.S.P.Q.2d 1321 (Fed. Cir. 2005) (*en banc*). One should rely *heavily* on the written description for guidance as to the meaning of the claims. *See id.* Moreover, interpretation of the claims must also be consistent with the interpretation that *one of ordinary skill in the art* would reach. *See In re Cortright*, 165 F.3d 1353, 1359, 49 U.S.P.Q.2d 1464, 1468 (Fed. Cir. 1999); M.P.E.P. § 2111.

Second, the burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). To establish a *prima facie* case, the Examiner must show, among other things, that the combination includes *all* of the claimed elements. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

Third, if the Examiner relies on a theory of inherency, the extrinsic evidence must make clear that the missing descriptive matter is *necessarily* present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *In re Robertson,* 169 F.3d 743, 49 U.S.P.Q.2d 1949 (Fed. Cir. 1999) (emphasis added). The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient. *Id.* In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art. *Ex parte Levy,* 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The Examiner, in presenting the inherency argument, bears the evidentiary burden and must adequately satisfy this burden. *See id.*

Deficiencies of the Cited References

Applicant respectfully submits that the cited references, taken alone or in hypothetical combination, do not disclose each and every recitation of the present claims. Indeed, embodiments of the present technique are directed to memory access, memory hierarchy and memory control strategies for use in embedded-DRAM digital signal processors (DSPs) and media processors. *See* Application, page 1, lines 8-11. In typical DSP and media processor applications, the processing of large data arrays stored in memory is required, typically requiring external memory. *See id.* at page 1, lines 16-20. To avoid delays in accessing external memory, large on-chip memories (or caches) have been utilized. *See id.* at page 1, lines 22-26. Typically, static random access memory (SRAM) has been utilized as the on-chip memory, but SRAM does not efficiently utilize chip area and may be cost prohibitive. *See id.* Accordingly, in some instances, dynamic random access memory (DRAM) has been integrated onto the same chip as the processor to interface with an SRAM cache. *See id.* at page 2, lines 25-26. This on-chip DRAM has used conventional instruction data caching structures, as well as direct memory access controllers to shuffle data between the on-chip

DRAM and the on-chip SRAM. *See id.* at page 2, line 28 to page 3, line 18. Conventional caching structures typically operate on a hit-or-miss basis and, thus, do not efficiently utilize the bandwith and wide data paths provided by DRAM. *See id.* at page 25, lines 10-20; page 30, lines 8-23. In contrast, embodiments of the present technique utilize intelligent caching that replaces conventional caching structures. *See id.* at page 30, lines 8-23. By utilizing the intelligent caching of the present technique, the wide data paths of the DRAM are utilized so that the amount of SRAM needed to provide the functional units with a constant source of data is minimized. *See id.*

Accordingly, the present independent claims recite methods and processors that utilize an embedded-DRAM processor architecture with a program controlled data transfer and caching structure that reduces or eliminates waiting time due to DRAM accessing. *See id.* page 4, lines 19-21. Specifically, independent claims 1, 13, 16, 23, 28, 45 and 50 each recite an embedded-DRAM processor that includes, in relevant part, "an *embedded DRAM array*." (Emphasis added). Further, independent claims 46, 48 and 49 each recite a method in a digital processor, the digital signal processor including, in relevant part, "an *embedded DRAM array*." Moreover, the claimed processors and/or methods also generally recite commands (or steps) for controlling the transfer of data between the DRAM array and the register files. By way of example, independent claims 1, 13, 46 and 48 generally recite separate commands to precharge a row of DRAM, deactivate the precharged row, and/or load elements (or columns) of the precharged row into one or more sets of data registers. By way of further example, independent claims 16, 28, 45, 49 and 50 generally recite the transfer of data from the DRAM array into a set of data registers that are in an inactive state.

The cited references do not disclose an embedded-DRAM array as recited in independent claims 1, 13, 16, 23, 28, 45, 46, 48, 49 and 50.

First, Applicant respectfully submits that the Inagami reference does not disclose an embedded-DRAM array, as recited in independent claims 1, 13, 16, 23, 28, 45, 46, 48, 49 and 50. As is clearly evident from Applicant's specification, an *embedded*-DRAM array is a DRAM array that is *integrated onto the same chip with the processor*. *See* Specification, page 2, line 25 to page 3, line 10; page 27, line 7-8; FIG. 1. In contrast, while the Inagami reference does disclose a vector processor having a main storage 1, the main storage 1 is not

integrated onto the same chip with the vector processor. *See* Inagami, col. 4, lines 15-17; FIG. 1. Indeed, nowhere does the Inagami reference disclose or suggest that the main storage 1 is on chip with the processor and, thus, embedded with the vector processor. As such, the Inagami reference clearly does not teach or suggest the claimed embedded-DRAM array.

The Examiner, however, is apparently asserting that the Inagami reference discloses an embedded-DRAM array because the main storage 1 is an integral part of the disclosed vector processor. *See* Office Action Mailed 04/05/06, page 46. Applicant notes that the Examiner is not giving an interpretation to the term "embedded" that is reasonable and consistent with the specification. Applicant emphasizes that the Examiner must interpret a claim recitation as one of ordinary skill in the art would reasonably interpret the claim in view of the specification. *See In re American Academy of Science Tech Center,* 70 U.S.P.Q.2d 1827 (Fed. Cir. 2004); *see also* M.P.E.P. § 2111 (describing the standards for claim interpretation during prosecution) (emphasis added). In the present rejection, the Examiner is apparently alleging that DRAM is embedded in a processor if it is an integral part of that processor. *See* Office Action Mailed 04/05/06, page 46. Specifically, the Examiner stated:

> Applicant is reading "embedded DRAM processor" too narrowly. Dictionary.com defines "embedded" in the following way: "To cause to be integral part of a surrounding whole." Clearly, in Fig. 1 of Inagami, the memory is an integral part of the overall processing system (processor). Hence, Inagami teaches an embedded DRAM processor.
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> *See id.*

The Examiner is apparently interpreting the word "embedded" independent of Applicant's specification and solely based on a definition obtained from an Internet source. Further, it would appear that the Examiner's interpretation would essentially read the term "embedded" out of the claims. Indeed, assuming the Examiner's interpretation is proper, the Examiner is giving no weight to the recitation of "embedded" because any memory that is present in a processing system would be an "integral part" of that processor. Thus, in accordance with this interpretation, the memory of any processing system is necessarily embedded. This is improper and not consistent with the specification, nor is it a reasonable interpretation that one of ordinary skill in the art would ascribe.

In view of the specification, an "embedded DRAM array" clearly refers to a DRAM array that is integrated onto the same chip as the processor. *See* Specification, page 2, line 25 to page 3, line 10; page 27, lines 7-8; FIG. 1. Indeed, the specification in the present application describes problems with accessing off-chip DRAM, requiring larger on-chip SRAM to avoid memory delays. *See id.* page 2, lines 8-24. To alleviate certain of these problems, DRAM may be placed onto the same chip as the processor. *See id.* page, 2, lines 25-26. Further, FIG. 1 describes an embedded-DRAM architecture with the DRAM arrays 102 integrated onto the same chip as the high-speed register files 112, 114 and 116 and the functional units 128. *See id.* page 22, lines 7-9; page 23, lines 3-5; page 27, lines 7-8; FIG. 1. For instance, the external interface 130 moves data on and off of the chip containing the DRAM arrays 102, the high-speed register files 112, 114 and 116 and the functional units 128. *See id.* page 27, lines 7-8; FIG. 1. Accordingly, the specification makes clear that embedded refers to the integration of the DRAM array *onto* the same chip as the processor.

Applicant therefore asserts that the Examiner's interpretation of an "embedded DRAM array" as memory that is an integral part of a processor is improper and is not the interpretation one of ordinary skill in the art would reach when reading the claims in view of the specification. Rather, as described above, one of ordinary skill in the art would understand that an "embedded DRAM array" refers to a DRAM array that is integrated onto the same chip as the processor, rather than the DRAM array simply being an integral part of the system as asserted by the Examiner. As the Inagami reference does not disclose a DRAM array that is integrated onto the same chip as the processor, it does not disclose each and every recitation of the present claims.

Accordingly, the Inagami reference does not disclose each and every feature recited in the present independent claims. Furthermore, the Examiner also relied on the Parady and Bissett references in the rejection of independent claims 16, 28, 45, 49 and 50. The Parady and Bissett references, however, do not remedy the deficiencies of the Inagami reference and, particularly, do not disclose an embedded DRAM array as recited in independent claims 16, 28, 45, 49 and 50. As such, the cited references, taken alone or in hypothetical combination, do not render obvious the present independent claims or the claims dependent therefrom

because the cited references do not disclose each and every feature recited in the present independent claims.

The cited references do not disclose separate commands to precharge, deactivate and/or load as generally recited in independent claims 1, 13, 46 and 48.

Furthermore, Applicant submits that the Inagami reference does not disclose an instruction set that includes separate commands to precharge a row of DRAM, deactivate the precharged row, and/or load elements (or columns) of the precharged row into one or more sets of data registers, as generally recited in independent claims 1, 13, 46 and 48. Indeed, the Examiner admits that Inagami reference is devoid of any disclosure of these recited commands. *See* Final Office Action Mailed 1/30/2007, page 4. The Examiner, however, is asserting that the recited precharging, deactivating and loading commands are inherently disclosed by the Inagami reference. Specifically, with respect to precharging and deactivating DRAM rows, the Examiner stated:

> b) Regarding the second argument, the examiner maintains the rejection. In order to read from a DRAM, the DRAM must be precharged (i.e., the DRAM must be activated). After a read occurs, the DRAM must be activated or else it will stay activated. Deactivation does not just occur on its own in a system, see Wright, column 1, lines 37-59, for further information.
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> c) Regarding the third argument, as the examiner pointed out, precharging DRAM is inherent. A DRAM is operating by precharging its bit lines to a value of VDD/2 volts. Then either 0 or 1 is read from the memory cell. A 1 will cause the VDD/2 value on the bit line to rise while a 0 will cause it to fall. A sense amp is then used to detect a rise or fall in the precharged value. And it is in this manner that a 0 or a 1 can be detected.
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> *See* Final Office Action Mailed 1/30/2007, page 48.

To the extent that the Examiner relies on a theory of inherency, the extrinsic evidence must make clear that the missing descriptive matter is *necessarily* present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. MPEP § 2112.IV; *see also In re Robertson,* 169 F.3d 743, 49 U.S.P.Q.2d 1949 (Fed. Cir. 1999). However, contrary to the Examiner's assertion, Applicant respectfully submits that it

is not necessarily true that the recited precharging, deactivating and loading would require separate commands. Indeed, the Wright reference relied on by the Examiner in support of this inherency argument makes clear that separate commands are not required. By way of example, the Wright reference contrasts synchronous DRAM (SDRAM) with asynchronous DRAM, in that SDRAM requires separate commands for precharging and accessing a row of storage cells while asynchronous DRAM does not require separate commands. *See* Wright, col. 1, lines 36-45. Therefore, separate commands for precharging, deactivating and loading clearly are not *necessarily* present in the Inagami reference, as the Wright reference clearly describes asynchronous DRAM as not having such separate commands.

Moreover, it is also not necessarily true that "the command to precharge is executed to precharge the row prior the command to load *so that at the time the command to load is issued, the command to load can execute without the need to wait for the row to precharge*," as recited in independent claim 13. (Emphasis added). Indeed, U.S. Patent No. 5,889,714 issued to Schumann et al. (hereafter referred to as "the Schumann reference") describes a drawback of DRAM as having a delay when accessing a row due to precharging. *See* Schumann, col. 1, lines 35-45. Specifically, the Schumann reference provides, "If a new access is to be made to a different row, a precharge operation must be completed to close the presently active row prior to accessing a different row. Therefore, a delay equal to the precharge time is experienced whenever a different row must be accessed on a subsequent transaction." *See id.* Accordingly, in certain instances, a command to load from conventional DRAM is not issued after the precharge command, but rather must wait until the row has been precharged. Accordingly, it is not necessarily true that the precharge command is executed prior to the execution of the load command so that the command to load can execute without the need to wait for the row to precharge, as recited in independent claim 13.

Accordingly, for this additional reason the Inagami reference does not render obvious independent claims 1, 13, 46 and 48 or the claims dependent therefrom because the Inagami reference does not disclose each and ever feature recited in the independent claims 1, 13, 46 and 48.

The cited references do not disclose register files that are capable of being placed into an inactive state as recited in independent claims 16, 28, 45, 49, and 50.

In addition, Applicant submits that the cited references do not disclose register files that are *capable of being placed into an inactive state*, as recited in independent claims 16, 28, 45, 49 and 50. With respect to this recitation, the Examiner stated:

> d) Inagami has not taught that each of said register files is also being capable of being placed into an active state and an inactive state. However, Parady has taught a thread switch command which performs such state toggling. More specifically, in Parady, every time a thread switch occurs, a new register file becomes active and the previously active register file becomes inactive. This allows for thread switching without having to save or reload a context of a thread, thereby saving processing time.
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> *See* Final Office Action Mailed 1/30/2007, page 23.

At the outset, Applicant notes that the Examiner is apparently not giving an interpretation to the term "inactive state" that is reasonable and consistent with the specification. Applicant understands that the Examiner is alleging that inactive register files are merely register files that are not currently being accessed by the functional units. *See id.* Applicant respectfully disagrees with the Examiner's interpretation of Applicant's recited term. Rather, in view of the specification and the plain language of the claim, an inactive register file is a deselected register file that is *not accessible* to the functional units. For example, independent claim 16 clearly states that "registers in the inactive state *are not accessible by the functional units.*" (Emphasis added). Moreover, with respect to this recitation, the present application provides:

> A programming model is presented wherein the functional units 128 perform arithmetic operations on data stored in one or more architectural register files. An architectural register file is a register file visible to the programmer, i.e., is a register file whose registers may be referenced as operands in instructions executed by the functional units 128. The selector 120 can switch different ones of the register files 112, 114, 116 to be the architectural register file. A selected register file is said to be an active register file. A deselected register file is not

> accessible to the functional units 128 and is said to be an inactive register file.
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> Application, page 24, lines 24-30.

Accordingly, an inactive register file is a deselected register file that is *not accessible* (as opposed to not being currently accessed) to the functional units. *See id.* Unlike the active register files that are visible to the programmer, the inactive register files are not visible to the programmer, i.e., the registers may not be referenced as operands in instructions executed by the functional units. *See id.*

Referring more specifically to the Examiner's rejection, the Examiner admitted that the Inagami reference does not disclose register files that are capable of being placed into an inactive state. *See* Final Office Action Mailed 1/30/2007 page 23. However, the Examiner has attempted to remedy the deficiencies of the Inagami reference by citing the Parady reference. *See id.* Applicant respectfully submits that the Parady reference cannot be used to obviate the deficiencies of the Inagami reference, in that it does not disclose inactive register files as recited in the present claims. Rather, the Parady reference is directed to a method and apparatus for switching between threads of a program in response to a long-latency event. *See* Parady, Abstract. Specifically, the Parady reference provides for switching between register files that are on different threads based on cache misses. *See id.* col. 3, lines 56-65. However, the register files that are not currently accessed after the thread switch has occurred are still accessible by the functional units, in that those register files are still visible to the programmer. As such, the thread switch does not toggle the register files to an inactive state as recited in the present claims, but merely switches the processing of a program to a different thread. The Parady reference, therefore, does not disclose each and every feature recited in independent claims 16, 28, 45, 49 and 50.

Furthermore, the Bissett reference cannot be used to remedy the deficiencies of the Inagami and Parady references. Indeed, the Bissett reference merely discloses the general concept that certain operations can be performed without influencing processor operation. *See* Bissett, col. 4, lines 3-9. The Bissett reference, however, does not disclose register files that are not accessible by functional units (i.e., in an inactive state), as generally recited in the

present claims. *See id.* As such, the cited references, taken alone or in hypothetical combination, do not render obvious independent claims 16, 28, 45, 49 and 50 because the cited references do not disclose each and every feature of the present independent claims.

The cited references do not disclose loading data into inactive register files as generally recited in independent claims 16, 28, 45, 49, and 50.

Furthermore, Applicant submits that the cited references do not disclose loading data into register files that are in an inactive state, as generally recited in independent claims 16, 28, 45, 49 and 50. Indeed, the Examiner admitted that neither the Inagami reference nor the Parady reference discloses this recitation. *See* Final Office Action Mailed 1/30/2007, page 24. However, the Examiner has attempted to remedy the deficiencies of the Inagami and Parady references by citing the Bissett reference. *See id.* Applicant respectfully submits that the Bissett reference cannot be used to obviate the deficiencies of the Inagami reference. Indeed, the Bissett reference merely discloses that certain operations do not influence software and do not need to be disabled. *See* Bissett, col. 4, lines 3-9. Such operations include background DMA, memory refresh, cache fills and writebacks, branch prediction, instruction prefetch, and data prefetch. *See id.* Nowhere, however, does the Bissett reference disclose that any of these operations involve the loading of data into a register file that is in an inactive state, which as described above, is a register file that cannot be accessed by a functional unit. *See id.* Nor is it clear that any of these operations would necessarily require the loading of data into an inactive register file. *See id.* Indeed, Applicant submits that certain of these operations may be performed on register files that are still accessible by the functional units, but are merely not currently being accessed. Therefore, the Bissett reference cannot remedy the deficiencies of the Inagami and Parady references because it does not disclose each and every recitation of the present claims. Accordingly, the cited references, taken alone or in hypothetical combination, do not render obvious independent claims 16, 28, 45, 49 and 50.

In view of the arguments set forth above, Applicant respectfully requests that the Examiner withdraw each of the rejections under 35 U.S.C. § 103 and provide an indication of allowance for all of the pending claims.

Remarks Regarding New Claim

Applicant has added new claim 51 which is dependent on claim 1. This new claim does not add any new matter. For the reasons discussed above and for additional reasons relating to other claim features, Applicant believes that this claim is patentable over the cited references and in condition for allowance. First, Applicant asserts, as discussed above regarding the Section 103 rejections, that the Inagami reference does not disclose all of the features recited in independent claim 1. For this reason alone, claim 51, which is dependent thereon, is also allowable. In addition, claim 51 recites features that are not disclosed in the Inagami reference. For example, claim 51 recites that "wherein each of said sets of registers is capable of being loaded or stored in response to a single latch signal *without a caching system that employs cache hits and cache misses*." (Emphasis added). Therefore, Applicant requests that the Examiner allow new claim 51.

General Authorization for Payment of Fees and Extensions of Time

Applicant does not believe that any fees are due; however, if any fees are due at this time or during the pendency of this application, the Commissioner is authorized to charge such requisite fees to Deposit Account No. 06-1315; Order No. MICS:0171-2. Furthermore, in accordance with 37 C.F.R. § 1.136, Applicant hereby provides a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefor and authorizes the Commissioner to charge any fees associated therewith to the above-referenced Deposit Account.

Conclusion

In view of the remarks and amendments set forth above, Applicant respectfully requests allowance of the pending claims. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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